AMENDMENTS TO THE CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (previously amended): In a method of etching a surface of a wafer with a microscopic roughness to prepare the wafer surface for receiving a deposition of a material on the wafer surface, the steps of

removing a thin layer from the surface of the wafer to eliminate any impurities from the surface of the wafer, and

thereafter creating the microscopic roughness on the surface of the wafer to receive a deposition of the material on the surface by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 2 (cancelled)

Claim 3 (currently amended): In a method as set forth in claim [[2]] [[1]] wherein

the inert gas is argon.

Claim 4 (previously presented): In a method as set forth in claim 1 wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland after the microscopic roughness has been produced on the surface of the wafer.

Claim 5 (previously presented): In a method of providing for an attachment of an electrical component to a wafer, the steps of:

removing a thin layer from the surface of the wafer,

thereafter depositing a chromium layer with a low intrinsic tensile stress on the cleaned surface of the wafer, and

thereafter depositing a layer of nickel vanadium with an intrinsic stress on the surface of the chromium layer to neutralize the low intrinsic tensile stress produced by the chromium layer.

Claim 6 (previously amended): In a method as set forth in claim 5 wherein

a microscopic roughness is produced on the surface of the wafer after the thin layer of the wafer has been removed from the surface of the wafer and wherein

the chromium layer is thereafter deposited on the microscopically rough surface of the wafer and wherein

a low rate of flow of an inert gas is provided on the wafer layer when the chromium layer is deposited on the surface of the wafer thereby to minimize the presence of the inert gas in the chromium layer.

Claim 7 (currently amended): In a method as set forth in claim 5 wherein

a waferland is disposed in an abutting relationship with the wafer and wherein

a layer of chromium is deposited on the surface of the waferland ~~before~~ after etching the surface of the wafer.

Claim 8 (previously presented): In a method as set forth in claim 5 wherein

the chromium layer is deposited on the surface of the wafer to produce an intrinsic tensile stress in the chromium layer and wherein

the nickel vanadium layer is deposited on the surface of the chromium layer with an RF bias power to produce an intrinsic compressive stress in the nickel vanadium layer.

Claim 9 (previously presented): In a method as set forth in claim 5 wherein

the chromium is deposited in a layer on the microscopically rough surface of the wafer to produce an intrinsic tensile stress with a low stress value in the chromium layer and wherein

the nickel vanadium layer is deposited on the surface of the chromium layer to produce a low intrinsic compressive stress with a value to neutralize the low intrinsic tensile stress in the chromium layer.

Claim 10 (previously presented): In a method as set forth in claim 7 wherein

the chromium is deposited in a layer on the microscopically rough surface of the wafer in an intrinsic tensile stress with a low stress value and wherein

the layer of the nickel vanadium is deposited on the surface of the chromium in an intrinsic compressive stress with a low stress value substantially neutralizing the low stress value of the intrinsic tensile stress of the chromium layer.

Claim 11 (previously presented): In a method of providing for an attachment of an electrical component to a wafer, the steps of:

removing a thin layer from the surface of the wafer, and

depositing a chromium layer with a low intrinsic tensile stress on the surface of the wafer after the removal of the thin layer from the surface of the wafer.

Claim 12 (previously presented): In a method as set forth in claim 11 wherein

the surface of the wafer is provided with a microscopic roughness after the thin layer has been removed from the surface of the wafer and wherein

the chromium layer is deposited on the microscopically rough surface of the wafer in an intrinsic tensile stress with a low stress value.

Claim 13 (previously presented): In a method as set forth in claim 11 wherein

the chromium layer is deposited on the surface of the wafer in a magnetron with no RF bias in the magnetron and with a low flow rate of molecules of an inert gas in the magnetron.

Claim 14 (previously presented): In a method as set forth in claim 11 wherein

a chamber is provided in which to perform the recited steps and wherein molecules of an inert gas flow through the chamber in an order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm).

Claim 15 (previously presented): In a method as set forth in claim 12 wherein

a chamber is provided in which to perform the recited steps and wherein

a waferland is disposed in the chamber to support the wafer and wherein a layer of chromium is deposited on the waferland before the chromium layer is deposited on the surface of the wafer.

Claim 16 (previously presented): In a method as set forth in claim 11 wherein

a waferland and a chamber are provided and the wafer and the waferland are disposed in the chamber and wherein

the chromium layer is deposited on the surface of the wafer in the chamber with no RF bias on the waferland in the chamber and with a low flow rate of molecules of an inert gas in the chamber,

the inert gas is argon and the flow rate of the molecules of the inert gas in the chamber is in the order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm).

Claim 17 (previously presented): In a method of providing for an attachment of an electrical component or sub-assembly to a wafer, the steps of:

removing a thin layer from the surface of the wafer,

depositing a layer of chromium on the surface of the wafer with a low intrinsic tensile stress, and

depositing a nickel vanadium layer on the surface of the chromium layer with an RF bias power to produce a low intrinsic compressive stress in the nickel vanadium layer for neutralizing the low intrinsic tensile stress in the chromium layer.

Claim 18 (previously presented): In a method as set forth in claim 17 wherein

a layer of metal selected from the group consisting of gold, silver and copper is deposited on the surface of the layer of nickel vanadium and wherein

the nickel vanadium layer has a low intrinsic compressive stress to neutralize the low intrinsic tensile stress in the chromium layer and any stress in the metal layer selected from the group consisting of gold, silver and copper.

Claim 19 (previously presented): In a method as set forth in claim 18 wherein

the electrical component is soldered to the layer of the metal selected from the group consisting of gold, silver and copper.

Claim 20. (currently amended) In a method as set forth in claim 18 wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland ~~before~~ after the thin layer is removed from the surface of the wafer and wherein

the electrical component is soldered to the layer of the metal selected from the group consisting of gold, silver and copper.

Claim 21 (previously presented): In a method as set forth in claim 20 wherein

a lens shield is disposed in a spaced relationship to the waferland and the lens shield is grounded and wherein

the RF bias power for the deposition of the layer of nickel vanadium is provided between the waferland and the grounded lens shield.

Claim 22 (previously presented): In a method of providing for an attachment of an electrical component to a wafer, the steps of:

removing a thin layer from the surface of the wafer,

thereafter providing the surface of the wafer with a microscopic roughness,

thereafter depositing a layer of chromium on the microscopically rough surface of the wafer with a low intrinsic tensile stress, and

thereafter depositing a layer of nickel vanadium on the surface of the wafer with a low intrinsic compressive stress.

Claim 23 (previously presented): In a method as set forth in claim 21 wherein

a layer of a metal selected from a group consisting of gold, nickel and copper is deposited on the surface of the nickel vanadium layer and wherein

a component is soldered to the layer of the metal selected from the group consisting of copper, gold and silver.

Claim 24 (previously presented): In a method as set forth in claim 23 wherein

the layer of the chromium is deposited on the microscopically rough surface of the wafer with no RF bias.

Claim 25 (previously presented): In a method as set forth in claim 22 wherein

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of the flow of an inert gas.

Claim 26 (previously presented): In a method as set forth in claim 24 wherein

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of flow of an inert gas and wherein

an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer to produce the low intrinsic compressive stress in the nickel vanadium layer.

Claim 27 (currently amended): In a method as set forth in claim 2[[1]] [[2]] wherein

the layer of the chromium is deposited on the microscopically rough surface of the wafer with no RF bias and wherein

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of flow of an inert gas and wherein

an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer to produce the low intrinsic compressive stress in the nickel vanadium layer.

Claim 28 (previously amended): In a method as set forth in claim 27 wherein

a layer of a metal selected from a group consisting of gold, nickel and copper is deposited on the surface of the nickel vanadium layer and wherein

the component is soldered to the layer of the metal selected from the group consisting of copper, gold and silver.

Claim 29 (previously presented): In a method of providing a deposition on a surface of a wafer, the steps of:

removing a thin layer from the surface of the wafer to eliminate impurities from the surface of the wafer,

creating a microscopic roughness on the surface of the wafer, and

depositing a chromium layer with a low intrinsic tensile stress on the microscopically rough surface of the wafer.

Claim 30 (previously presented): In a method as set forth in claim 29 wherein

the chromium layer is deposited on the microscopically rough surface of the wafer in a chamber and wherein

an inert gas having a low flow rate is passed through the chamber with no RF bias on the wafer, when the chromium layer is deposited on the microscopically rough surface of the wafer, to prevent molecules of the inert gas from being entrapped in the chromium layer.

Claim 31 (previously amended): In a method as set forth in claim 30 wherein

the inert gas is argon.

Claim 32 (previously presented): In a method as set forth in claim 30 wherein

the microscopic roughness is produced on the surface of the wafer by providing the molecules of the inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 33 (previously presented): In a method as set forth in claim 29 wherein

no RF bias is provided when the chromium layer is deposited on the surface of the wafer and wherein

the chromium layer is deposited on the microscopically rough surface of the wafer in a chamber and wherein

an inert gas having a low flow rate is passed through the chamber, when the chromium layer is deposited on the microscopically rough surface of the wafer, to prevent the inert gas from being entrapped in the chromium layer and wherein

the inert gas is argon.

Claim 34 (previously presented): In a method as set forth in 31 wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland, before etching the wafer surface, to prevent the layer of chromium deposited on the wafer from being contaminated by the material from the waferland.

Claim 35 (previously presented): In a method of preparing a wafer surface for receiving an electronic component, the steps of:

removing a thin layer from the surface of the wafer,

thereafter creating a microscopic roughness on the surface of the wafer by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer, and

thereafter depositing a chromium layer on the microscopically rough surface of the wafer in a chamber in which a minimal amount of an inert gas is passed through the chamber during the deposition to prevent molecules of the inert gas from being entrapped in the chromium layer.

Claim 36 (previously presented): In a method as set forth in claim 35 wherein

no wafer bias is produced on the wafer when the chromium layer is deposited on the surface of the wafer.

Claim 37 (previously presented): In a method as set forth in claim 35 wherein

the chromium layer is deposited on the surface of the wafer under tension with a low amount of stress.

Claim 38 (previously presented): In a method as set forth in claim 36 wherein

the chromium layer is deposited on the surface of the wafer with a low amount of intrinsic tensile stress.

Claim 39 (previously presented): In a method of providing a deposition on a surface of a wafer for receiving an electronic component on the wafer surface, the steps of:

removing a thin layer from the surface of the wafer,

creating a microscopic roughness on the surface of the wafer, and

atomically bonding a chromium layer to the microscopically rough surface on the wafer.

Claim 40 (previously presented): In a method as set forth in claim 39 wherein

the chromium layer is deposited on the microscopically rough surface of the wafer with no RF bias.

Claim 41 (previously presented): In a method as set forth in claim 39, the step of:

providing a low intrinsic tensile stress in the chromium layer.

Claim 42 (previously presented): In a method as set forth in claim 39 wherein

the microscopic roughness on the surface of the wafer is provided by disposing the wafer in a chamber and by passing ions of an inert gas through the chamber with insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 43 (currently amended): In a method as set forth in claim 40 wherein

~~providing~~ an intrinsic tensile stress is provided with a low value in the chromium layer and wherein

the microscopic roughness on the surface of the wafer is provided by disposing the wafer in a chamber and by passing ions of an inert gas through the chamber with insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 44 (previously presented): In combination for performing electrical functions,

a wafer having a clean surface with a microscopic roughness, and

a layer of chromium deposited on the microscopically rough surface of the wafer with a low intrinsic tensile stress in the chromium layer.

Claim 45 (previously presented): In a combination as set forth in claim 44 wherein

the chromium layer is deposited on the microscopically rough surface of the wafer with a low intrinsic tensile stress at a rate of flow of an inert gas in the order of 3-5 SCCM.

Claim 46 (previously presented): In a combination as set forth in claim 44 wherein

the microscopic roughness is provided on the surface of the wafer by ions of an inert gas with an insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 47 (previously presented): In a combination as set forth in claim 44 wherein

an atomic bonding is produced between the chromium in the chromium layer and the microscopically rough surface of the wafer.

Claim 48 (previously presented): In combination for performing electrical functions,

a wafer,

a chromium layer deposited on the wafer with a low intrinsic tensile stress, and

a layer of nickel vanadium deposited on the chromium layer in firmly adhered relationship to the chromium layer with a low intrinsic compressive stress.

Claim 49 (previously presented): In a combination as set forth in claim 48,

the chromium layer being under the low intrinsic tensile stress and the nickel vanadium layer being under the low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer.

Claim 50 (currently amended): In a combination as set forth in claim 48,

~~the chromium in the chromium layer having the low intrinsic tensile stress for bonding to the microscopically rough wafer surface,~~

the chromium in the chromium layer having a low intrinsic tensile stress and an atomic bonding with the microscopically rough surface on the wafer.

Claim 51 (previously presented): In combination for performing electrical functions,

a wafer having a clean surface with a microscopic roughness, and

a chromium layer deposited on the microscopically rough surface of the wafer and atomically bonded to the microscopically rough wafer surface.

Claim 52 (previously presented): In a combination as set forth in claim 51,

the chromium layer having a low intrinsic tensile stress for bonding to the microscopically rough wafer surface.

Claim 53 (previously presented): In combination for performing electrical functions,

a wafer having a clean surface,

a chromium layer disposed on the clean surface of the wafer with an intrinsic tensile stress, and

a nickel vanadium layer deposited on the chromium layer with a low intrinsic compressive stress.

Claim 54 (previously presented): In a combination as set forth in claim 53 wherein

the low intrinsic compressive stress of the nickel vanadium layer substantially neutralizes the low intrinsic tensile stress of the chromium layer.

Claim 55 (previously presented): In a combination as set forth in claim 53 wherein

the clean surface of the wafer has a microscopic roughness and wherein

the chromium in the chromium layer is atomically bonded to the microscopically rough surface of the wafer.

Claim 56 (currently amended): In a combination as set forth in claim 5[[2]] [[3]],

a layer of a metal selected from the group consisting of copper, gold and silver and disposed on the nickel vanadium layer with a low intrinsic tensile stress.

Claim 57 (previously presented): In a combination as set forth in claim 53 wherein

a layer of a metal selected from the group consisting of copper, gold and silver is deposited on the nickel vanadium layer and wherein

the nickel vanadium layer substantially neutralizes any intrinsic stress in the metal layer selected from the group consisting of copper, gold and silver.

Claim 58 (previously presented): In a combination as set forth in claim 53 wherein

an electrical component is soldered to the layer of the metal selected from the group consisting of copper, gold and silver.

Claim 59 (previously amended): In a method of etching a surface of a wafer with a microscopic roughness, the steps of:

providing a flow of an inert gas in the order of forty (40) to fifty (50) standard cubic centimeters per minute through a chamber containing the wafer and at a relatively high gas pressure in the order of 4-6 10^{-3} Torrs to remove a thin layer from the surface of the wafer,

thereafter providing a flow of an inert gas through the chamber at a flow rate of approximately forty (40) to fifty (50) standard cubic centimeters per minute and a power in the order of six hundred watts (600 W) to twelve hundred watts (1200 W) to remove impurities from the surface of the wafer and provide an anatomically rough surface,

disposing the wafer on a waferland, and

then providing a flow of an inert gas at a rate of approximately 40-50 standard cubic centimeters per minute through the chamber at a low power in the order of fifty watts (50 W) to one hundred watts (100 W) to provide the surface of the wafer with the microscopic roughness.

Claim 60 (previously amended): In a method as set forth in claim 59 wherein

the power applied in the chamber to remove the impurities from the surface of the wafer is in the order of 600-1200 watts for approximately thirty (30) seconds and wherein

the flow of the inert gas through the chamber to provide the surface of the wafer with the microscopic roughness occurs for a period of approximately sixty (60) seconds.

Claim 61 (previously presented): In a method as set forth in claim 59 wherein

a layer of chromium is deposited on the microscopically rough surface of the wafer without any RF bias and at a low flow rate of the inert gas.

Claim 62 (previously presented): In a method as set forth in claim 59 wherein

a layer of nickel vanadium is deposited on the surface of the chromium layer with an RF bias power of approximately 300 watts and with a flow rate of argon of approximately 5 sccm.

Claim 63 (previously presented): In a method as set forth in claim 60 wherein

a layer of chromium is deposited on the surface of the waferland before the surface of the wafer is etched.

Claim 64 (previously amended): In a method as set forth in claim 60 wherein

the nickel vanadium layer is deposited on the chromium layer with a power of approximately six thousand watts (6000 W), with a flow rate of argon of approximately five (5) sccm and with RF power of approximately three hundred (300) watts.

Claim 65 (previously presented): In a method as set forth in claim 29 wherein

the chromium layer is deposited with a low intrinsic tensile stress on the microscopically rough surface by providing the layer with no RF bias.

Claim 66 (previously presented): In a method as set forth in claim 29 wherein

the microscopic roughness is created on the surface of the wafer by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 67 (previously amended): In a method as set forth in claim 1 wherein

the inert gas is argon and wherein

the wafer is disposed on a waferland and wherein

a layer of chromium is deposited on the waferland after the microscopic roughness has been produced on a the surface of the wafer.

Claim 68 (previously presented): In a method as set forth in claim 22 wherein

the microscopic roughness on the surface of the layer is created by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 69 (previously presented): In a method as set forth in claim 39 wherein

the microscopic roughness is created on the surface of the wafer by

providing ions of an inert gas on the surface of the wafer with an

insufficient energy to etch the surface of the wafer but a sufficient energy to create the microscopic roughness on the surface of the wafer.

REMARKS

1. Claims 1 and 3-69 have been retained in the application. Claim 3 has been amended to make it dependent from claim 1. A minor change has also been made in claim 68. The other claims have not been amended.

2. Claims 1 and 3 have been rejected under 35 U.S.C. 102(a) as being clearly anticipated by Ueno patent 6,294,444. Claims 1 and 3 are allowable over Ueno because Ueno does not disclose the step of creating microscopic roughness on the surface of the wafer to receive a deposition of the material on the surface by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

The Examiner had indicated in the Office Action dated 11/17/2004 that Ueno discloses the recitation specified in the previous paragraph. The Examiner has cited Col. 1, lines 60 and 67 and Col. 2, lines 1-38. Applicant's attorney has studied this portion in Ueno and does not find any disclosure in Ueno corresponding to what is recited in claim 1. Applicant would appreciate it if the Examiner would specify a particular column and line in Ueno (and not forty (40) lines) where Ueno discloses this.

3. Claim 4 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno as applied to claim 1 and further in view of Hong (U.S. 6,375,810) and Hori (U.S. 6,399,411).

Claim 4 is allowable over the cited references for the same reasons as claim 1 because it is dependent from claim 1. Actually, none of the Ueno, Hong and Hori

discloses the recitation in claim 1. Claim 4 is also allowable over the references because it recites that wafer is deposited on a waferland and that the layer of chromium is deposited on the waferland after the microscopic roughness has been produced on the surface of the wafer. None of the references discloses that a layer of chromium is deposited on the waferland after the microscopic roughness has been produced on the surface of the wafer.

4. Claims 5-20, 22-58 and 65-69 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno and Hong as applied to claims 1 and 4 above and further in view of Stress Control in Multi-layer Backride Metalization of Thinned Wafers (TW article), the Admitted Prior Art and Tailoring Sputtered or cr Films on Large Wafer Article (LW article).

Applicant notes that the Examine has had to cite five (5) references in combination to reject each of claims 5-20, 22-58 and 65-69. If the methods recited in these claims are obvious to a person of ordinary skill in the art, why has the Examiner had to cite five (5) references in combination? If anything, the citation of five (5) references in combination shows that the claims are allowable. A person of ordinary skill in the art would not know of the five (5) references and (even if he knew of the references) would not understand that he could combine the references to provide the method steps recited in the claims.

The Examiner has cited Ueno against claims 5, 7, 9-12, 15, 17, 20, 22, 29, 32, 54, 35, 39, 42-44, 46-55 and 66-69. According to the Examiner, Ueno creates a microscopic roughness as the surface of the wafer by providing ions of an inert gas (i.e. argon) with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create a

microscopic roughness on the surface of the wafer. As applicant has previously indicated, Ueno does not provide any such disclosure. Applicant has invited the Examiner to cite the specific column and line where Ueno discloses this.

The Examiner has then cited Hong and has attempted to combine Ueno and Hong. However, the Examiner has admitted the following on page 5 of the Office Action dated 11/17/04.

> "Ueno-Hong discloses the claimed invention except thereafter depositing a chromium layer with a low intrinsic tensile stress on the cleaned surface of the wafer with a low stress value and thereafter depositing a layer of nickel vanadium with an intrinsic stress on the surface of the chromium layer to neutralize the low intrinsic tensile stress produced by the chromium layer."

The Examiner then indicates that the TW article "discloses depositing (i.e., atomically bonding) a chromium layer with a low intrinsic tensile stress on the cleaned surface of the wafer with a RF bias power and thereafter depositing a layer of nickel vanadium with an intrinsic stress on the surface of the chromium layer to neutralize the low intrinsic tensile stress produced by the chromium layer (see pages 4-15)."

The TW article does not disclose what the Examiner has stated in the quotation in the previous paragraph. The TW article discloses titanium, not chromium, as the material on which the nickel vanadium layer is deposited. Furthermore, the titanium deposited produced a compressive force in the TW article rather than a tensile force as with chromium. The wafer deposition in the TW article also had heat applied at 400°C to obtain good cohesion of the different layers. (Page 4, 2d paragraph or TW). The

titanium layer had to be deposited with a deep compression stress of about 8E9 dynes/cm^2, Page 13, lines 3 and 4 of the articles. In contrast, the chromium layer in the patent application has a tensile stress of a low magnitude and is deposited on a microscopically rough surface of the wafer. The TW article also does not disclose that the titanium layer is deposited on a microscopically rough surface of the wafer.

Claims 5, 7, 9-12, 15, 17, 20, 22, 29, 32, 34, 35, 39, 42-44, 46-55 and 66-69 are allowable over the combination of Ueno, Hong, the Admitted Prior Art and the TW article for the following reasons (LW is not cited against these claims):

Claim 5

depositing a chromium layer with a low intrinsic stress on the cleaned surface of the wafer, and

thereafter depositing a layer of nickel vanadium with an intrinsic stress on the surface of the chromium layer to neutralize the low intrinsic tensile stress produced by the chromium layer.

Claim 7

dependent from allowable claim 5

a layer of chromium is deposited on the surface of the waferland before etching the surface of the wafer

none of the references discloses that the layer of chromium is deposited on the surface of the waferland before etching the surface of the wafer.

Claim 9

dependent from allowable claim 5

the chromium is deposited in a layer on the microscopically rough surface of the wafer to produce an intrinsic tensile stress with a low stress value in the chromium layer and

the nickel vanadium layer is deposited on the surface of the chromium layer to produce a low intrinsic compressive stress with a value to neutralize the low intrinsic tensile stress in the chromium layer.

Claim 10

dependent from allowable claim 7

the chromium is deposited in a layer on the microscopically rough surface of the wafer in an intrinsic tensile stress with a low stress value and

the layer of the nickel vanadium is deposited on the surface of the chromium in an intrinsic compressive stress with a low stress value substantially neutralizing the low stress value of the intrinsic tensile stress of the chromium layer.

Claim 11

dependent from allowable claim 10

depositing a chromium layer with a low intrinsic tensile stress on the surface of the wafer after the removal of the thin layer from the surface of the wafer.

Claim 12

dependent from allowable claim 11

the chromium layer is deposited on the microscopically rough surface of the wafer in an intrinsic tensile stress with a low stress value.

Claim 15

dependent from allowable claim 12

a waferland is disposed in the chamber to support the wafer and a layer of chromium is deposited on the waferland before the chromium layer is deposited on the surface of the wafer.

Claim 17

depositing a layer of chromium on the surface of the wafer with a low intrinsic tensile stress, and

depositing a nickel vanadium layer on the surface of the chromium layer with an RF bias power to produce a low intrinsic compressive stress in the nickel vanadium layer for neutralizing the low intrinsic tensile stress in the chromium layer.

Claim 20

dependent from allowable claim 18

a layer of chromium is deposited on the waferland after the thin layer is removed from the surface of the wafer.

Claim 22

providing the surface of the wafer with a microscopic roughness,

thereafter depositing a layer of chromium on the microscopically rough surface of the wafer with a low intrinsic tensile stress, and

thereafter depositing a layer of nickel vanadium on the surface of the wafer with a low intrinsic compressive stress.

Claim 29

creating a microscopic roughness on the surface of the wafer and

on the microscopically rough surface of the wafer.

Claim 32

dependent from allowable claim 30

the microscopic roughness is produced on the surface of the wafer by providing the molecules of the inert gas with an insufficient energy to etch the surface of

the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 34

dependent from allowable claim 31

a layer of chromium is deposited on the waferland, before etching the wafer surface, to prevent the layer of chromium deposited on the wafer from being contaminated by the material from the waferland.

Claim 35

thereafter creating a microscopic roughness on the surface of the wafer by providing ions of an inert gas with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer, and

thereafter depositing a chromium layer on the microscopically rough surface of the wafer in a chamber in which a minimal amount of an inert gas is passed through the chamber during the deposition to prevent molecules of the inert gas from being entrapped in the chromium layer.

Claim 39

creating a microscopic roughness on the surface of the wafer, and

atomically bonding a chromium layer to the microscopically rough surface on the wafer.

Claim 42

dependent from allowable claim 39

the microscopic roughness on the surface of the wafer is provided by disposing the wafer in a chamber and by passing ions of an inert gas through the chamber with insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 43

dependent from allowable claim 40

providing an intrinsic tensile stress with a low value in the chromium layer and

the microscopic roughness on the surface of the wafer is provided by disposing the wafer in a chamber and by passing ions of an inert gas through the chamber with insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 44

a wafer having a clean surface with a microscopic roughness, and

a layer of chromium deposited on the microscopically rough surface of the wafer with a low intrinsic tensile stress in the chromium layer.

Claim 46

dependent from allowable claim 44

the microscopic roughness is provided on the surface of the wafer by ions of an inert gas with an insufficient energy to etch the surface of the wafer but with sufficient energy to produce the microscopic roughness on the surface of the wafer.

Claim 47

dependent from allowable claim 44

an atomic bonding is produced between the chromium in the chromium layer and the microscopically rough surface of the wafer.

Claim 48

a chromium layer deposited on the wafer with a low intrinsic tensile stress, and

a layer of nickel vanadium deposited on the chromium layer in firmly adhered relationship to the chromium layer with a low intrinsic compressive stress.

Claim 49

dependent from allowable claim 48

the chromium layer being under the low intrinsic tensile stress and the nickel vanadium layer being under the low intrinsic compressive stress to neutralize the low intrinsic tensile stress of the chromium layer.

Claim 50

dependent from allowable claim 48

the chromium in the chromium layer having the low intrinsic tensile stress for bonding to the microscopically rough wafer surface,

the chromium in the chromium layer having an atomic bonding with the microscopically rough surface on the wafer.

Claim 51

a wafer having a clean surface with a microscopic roughness, and

a chromium layer deposited on the microscopically rough surface of the wafer and atomically bonded to the microscopically rough wafer surface.

Claim 52

dependent from allowable claim 51

the chromium layer having a low intrinsic tensile stress for bonding to the microscopically rough wafer surface.

Claim 53

a chromium layer disposed on the clean surface of the wafer with an intrinsic tensile stress, and

a nickel vanadium layer deposited on the chromium layer with a low intrinsic compressive stress.

Claim 54

dependent from allowable claim 53

the low intrinsic compressive stress of the nickel vanadium layer substantially neutralizes the low intrinsic tensile stress of the chromium layer.

Claim 55

dependent from allowable claim 53

the chromium in the chromium layer is atomically bonded to the microscopically rough surface of the wafer.

Claim 66

dependent from allowable claim 29

the microscopic roughness is created on the surface of the wafer by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 67

dependent from allowable claim 1

a layer of chromium is deposited on the waferland after the microscopic roughness has been produced on a the surface of the wafer.

Claim 68

dependent from allowable claim 22

the microscopic roughness on the surface of the layer is created by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but with a sufficient energy to create the microscopic roughness on the surface of the wafer.

Claim 69

dependent from allowable claim 37

the microscopic roughness is created on the surface of the wafer by providing ions of an inert gas on the surface of the wafer with an insufficient energy to etch the surface of the wafer but a sufficient energy to create the microscopic roughness on the surface of the wafer.

5. Although claims 6, 8, 13, 14, 16, 24-27, 30, 31, 33, 36-38, 40, 41, 45 and 65 are included in the group in Section 4 of the REMARKS, they are discussed separately on page 6 of the Office Action dated 11/17/2005. Applicant accordingly discusses these claims as a separate group.

Applicant respectfully submits that the Examiner has made some misstatements in the paragraph on page 6, lines 3-12 of the Office Action dated 11/17/2004. For example, the Examiner has indicated that the TW article discloses on pages 4-15 and in Tables 1 and 2 that "molecules of an inert gas argon flow through the chamber in an order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm) in an environment of (5-15 sccm)." Applicant has not been able to find such a flow rate of argon on pages 4-15 of the TW article. Applicant would appreciate if the Examiner would specify by page and line where this disclosure in the TW reference. Applicant should also like to reiterate again that the TW reference discusses a deposition of a titanium layer, not a chromium layer.

The Examiner has also made the following statement on page 6 of the TW reference:

> "Thus, the chromium is deposited on the wafer at a low rate of flow of an inert gas and wherein the RF bias power during the deposition of the nickel vanadium layer on the chromium layer on the chromium layer to produce the low intrinsic compressive stress in the nickel vanadium layer."

As previously indicated, the TW article does not disclose a deposition of a nickel vanadium layer on a chromium layer. Furthermore, there is no discussion in the TW article of a production of an RF bias during the deposition of the nickel vanadium layer as the titanium layer. Applicant would appreciate if the Examiner would cite by page and line where the TW reference discusses the application of an RF bias during the deposition of the nickel vanadium layer on the chromium layer or even during the deposition of the nickel vanadium layer on a titanium layer. Applicant also respectfully submits that the LW article is not pertinent because it does not disclose the deposition of a chromium layer on a waferland after the microscopic roughness is produced on the surface of the wafer.

Claims 6, 8, 13, 14, 16, 24-27, 30, 31, 33, 36-38, 40, 41, 45 and 65 are allowable over the combination of Ueno, Hong, the TW article, the LW article and the Admitted Prior Art because of the following recitations:

Claim 6

dependent from allowable claim 5

a microscopic roughness is produced on the surface of the wafer after the thin layer of the wafer has been removed from the surface of the wafer and

the chromium layer is thereafter deposited on the microscopically rough surface of the wafer and

a low rate of flow of an inert gas is provided on the wafer layer when the chromium layer is deposited on the surface of the wafer thereby to minimize the presence of the inert gas in the chromium layer.

Claim 8

dependent from allowable claim 5

the chromium layer is deposited on the surface of the wafer to produce an intrinsic tensile stress in the chromium layer and

the nickel vanadium layer is deposited on the surface of the chromium layer with an RF bias power to produce an intrinsic compressive stress in the nickel vanadium layer.

Claim 13

dependent from allowable claim 11

the chromium layer is deposited on the surface of the wafer in a magnetron with no RF bias in the magnetron and with a low flow rate of molecules of an inert gas in the magnetron.

Claim 14

dependent from allowable claim 11

a chamber is provided in which to perform the recited steps and

molecules of an inert gas flow through the chamber in an order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm).

Claim 16

dependent from allowable claim 11

the chromium layer is deposited on the surface of the wafer in the chamber with no RF bias on the waferland in the chamber and with a low flow rate of molecules of an inert gas in the chamber,

the inert gas is argon and the flow rate of the molecules of the inert gas in the chamber is in the order of three (3) to five (5) standard cubic centimeters per minute (3-5 sccm).

Claim 24

dependent from allowable claim 23

the layer of chromium is deposited on the microscopically rough surface of the wafer with no RF bias.

Claim 25

dependent from allowable claim 22

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of the flow of an inert gas.

Claim 26

dependent from allowable claim 24

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of flow of an inert gas and

an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer to produce the low intrinsic compressive stress in the nickel vanadium layer.

Claim 27

dependent from allowable claim 21

the layer of the chromium is deposited on the microscopically rough surface of the wafer with no RF bias and wherein

the layer of chromium is deposited on the microscopically rough surface of the wafer at a low rate of flow of an inert gas and wherein

an RF bias power is applied during the deposition of the nickel vanadium layer on the chromium layer to produce the low intrinsic compressive stress in the nickel vanadium layer.

Claim 30

dependent from claim 29

the chromium layer is deposited on the microscopically rough surface of the wafer in a chamber and

an inert gas having a low flow rate is passed through the chamber with no RF bias on the wafer, when the chromium layer is deposited on the microscopically rough surface of the wafer, to prevent molecules of the inert gas from being entrapped in the chromium layer.

Claim 31

dependent from allowable claim 30.

Claim 33

dependent from allowable claim 29

the chromium layer is deposited on the microscopically rough surface of the wafer in a chamber and an inert gas having a low flow rate is passed through the chamber, when the chromium layer is deposited on the microscopically rough surface of the wafer, to prevent the inert gas from being entrapped in the chromium layer and the inert gas is argon.

Claim 36

dependent from allowable claim 35

no wafer bias is produced on the wafer when the chromium layer is deposited on the surface of the wafer.

Claim 37

dependent from allowable claim 35

the chromium layer is deposited on the surface of the wafer under tension with a low amount of stress.

Claim 38

dependent from allowable claim 36

the chromium layer is deposited on the surface of the wafer with a low amount of intrinsic tensile stress.

Claim 40

dependent from allowable claim 39

the chromium layer is deposited on the microscopically rough surface of the wafer with no RF bias.

Claim 41

dependent from allowable claim 39

providing a low intrinsic tensile stress in the chromium layer.

Claim 45

dependent from allowable claim

the chromium layer is deposited on the microscopically rough surface of the wafer with a low intrinsic tensile stress at a rate of flow of an inert gas in the order of 3-5 SCCM.

Claim 65

dependent from allowable claim 29

the chromium layer is deposited with a low intrinsic tensile stress on the microscopically rough surface by providing the layer with no RF bias.

6. The Examiner has rejected claims 18, 19, 23, 28 and 56-58 as obvious in view of the combination of Ueno, Hong, the TW article, the Admitted Prior Art and the LW article. Claims 18, 19, 23, 28 and 50-58 are allowable over this combination of references because of the following recitations:

Claim 18

dependent from allowable claim 17

the nickel vanadium layer has a low intrinsic compressive stress to neutralize the low intrinsic tensile stress in the chromium layer and any stress in the metal layer selected from the group consisting of gold, silver and copper.

Claim 19

dependent from allowable claim 18.

Claim 23

dependent from allowable claim 21.

Claim 28

dependent from allowable claim 27.

Claim 56

dependent from allowable claim 53

Claim 57

dependent from allowable claim 53

the nickel vanadium layer substantially neutralizes any intrinsic stress in the metal layer selected from the group consisting of copper, gold and silver.

Claim 58

dependent from allowable claim 53

7. In order for different prior art references to be combined to reject a claim, the references have to disclose or suggest the combination recited in the claim ACS Hospitality Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984). As the Federal Circuit indicated in the ACS case at 732 F2d. 1577, 1579, 221 USPQ 929, 933:

> "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. Under Section 103, teaching of references can be combined only if there is some suggestion or incentive to do so."

See also In re Fine, 837 F.2d 1071, 5 USPQ 2d 1596 (Fed. Cir. 1988) and Janice Jones, 1958 F.2d 347, 21 USPQ 2d 1941 (Fed. Cir. 1992) in support of the holding in the ACS case.

None of the references cited by the Examiner to reject the claims in this application discloses or suggests certain of the features recited in the claims. This has

been discussed in considerable detail above. The references cannot accordingly be combined to reject the claims. This applies to all of the claims.

8. Claims 1 and 3-69 are allowable over the cited references for the reasons discussed above in detail.

The Commissioner is authorized to charge any deficiencies in fees or credit any overpayments to our Deposit Account No. 06-2425.

Respectfully submitted,

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